WHAT IS CLAIMED IS:

1. A discrete cosine transformation apparatus comprising:

a transposition section which transposes data between a one-dimensional processing and a two-dimensional processing in every N pixels of an input picture signal of N × N pixels to produce a transposed output; and

a transformation section which subjects the transposed output of the transposition section to a discrete cosine transformation.

2. The discrete cosine transformation apparatus according to claim 1, wherein the transposition section transposes the picture signal of 8 × 8 pixels in every eight pixels.

3. The discrete cosine transformation apparatus according to claim 2, further comprising:

an input processor which outputs data input in units of L, at a rate of 2M2L data per clock period for $4(N/M) \cdot N/2L$ periods and which, for the succeeding $4(N/M)$ periods, selects and outputs data output at 2M data per clock period from the transposition section to the transformation section.

4. The discrete cosine transformation apparatus according to claim 3, wherein the transposition section has a transposition memory in which N × N data are written at the rate of 2M data per clock period for

4(N/M)·N/2L periods, then transposed, and read out at the rate of 2M data per clock period for four clock periods.

5. The discrete cosine transformation apparatus according to claim 1, further comprising a control section which produces control signals including a first signal and a second signal, the first signal being for limiting in every N/M clock periods the timing of starting the fetch of data input at the input terminal when the input of all the one-dimensional transformed data to the transformation section is not completed, but not limiting the timing of starting the fetch of data input to the input terminal when all the one-dimensional transformed data is completely input to the transformation section, and the second signal being indicative of a head of output block data.

6. An inverse discrete cosine transformation apparatus comprising:

a transposition section which transposes input DCT coefficients of N × N in every N coefficients between one-dimensional processing and two-dimensional processing; and

a transformation section which subjects an output of the transposition section to an inverse discrete cosine transformation.

7. An inverse discrete cosine transformation apparatus according to claim 6, wherein

the transposition section transposes the picture signal of 8 × 8 pixels in every eight pixels.

8. An inverse discrete cosine transformation apparatus according to claim 6, further comprising:

an input processor which outputs first data input one by one, at a rate of two units of data per clock period for four clock periods and which, for the succeeding four clock periods, selects and outputs second data output at two units of data per clock period from the transposition section to the transformation section.

9. A discrete cosine transformation/inverse discrete cosine transformation apparatus comprising:

a single N-point transformation processor which switches in every N points between the one-dimensional processing and the two-dimensional processing to perform orthogonal transformation of N × N points.

10. A discrete cosine transformation/inverse discrete cosine transformation apparatus according to claim 9, wherein the N-point transformation processor incorporates a single eight-pixel transformation processor which switches in every eight pixels between one-dimensional processing and two-dimensional processing to perform orthogonal transformation of 8 × 8 pixels.

11. A discrete cosine transformation/inverse discrete cosine transformation apparatus according to

claim 10, further comprising an input processor which comprises an input register configured to fetch in every clock period the data input from a first input terminal, a selector which is responsive to a control signal input from a second terminal and shifts an output of the input register three bits to the left for the discrete cosine transformation because the lower nine bits of the input data are valid and for directly outputting the output of the register without carrying out any bits shifting for the inverse discrete cosine transformation, a plurality of stage registers which are responsive to a control signal input from a third input terminal, update the data in every clock periods and saves it for five clock periods, a selector which is responsive to a control signal input from a fourth input terminal and outputs the data saved in the registers in an reverse of the input sequence, a selector which is responsive to a control signal input from the third input terminal, selects an output of the shifter and an output of the selector in every four clock periods, and outputs at a rate of two units of data per clock period eight units of data input at a rate of one data per clock period from the first input terminal for four clock periods and at the rate of two units of data per clock period transposed data input from the fourth input terminal for the succeeding four clock periods, and a selector which is responsive

to a control signal input from a fifth input terminal and interchanges the data so that its sequence is suited for the arithmetic operation in the eight-pixel transformation processor.

12. A discrete cosine transformation/inverse discrete cosine transformation apparatus according to claim 10, wherein the eight-pixel transformation processor comprises a first addition/subtraction processor for the discrete cosine transformation, a sum-of-products processor and a second addition/subtraction processor for the inverse discrete cosine transformation,

the first addition/subtraction processor includes a section which generates a discrete cosine intermediate signal of the pixel data input from the input terminal for the discrete cosine transformation and directly outputs the discrete cosine coefficients input from the input terminal with one of inputs of the adder controlled to zero for the inverse cosine transformation,

the sum-of-products processor includes a section which subjects the input discrete cosine intermediate signal to a sum-of-products operation to output a transformed result for the discrete cosine transformation and subjects the input discrete cosine transform coefficients to a sum-of-products operation to output a transformation intermediate signal, and

the second addition/subtraction processor includes a section which generates a real signal as the transformed result from the inverse discrete cosine intermediate signal for the inverse discrete cosine transformation and directly outputs the input data with one of inputs of the adder controlled to zero for the discrete cosine transformation.

13. The discrete cosine transformation/inverse discrete cosine transformation apparatus according to claim 10, further comprising an output processor which comprises a first selector configured to interchange the data input at the rate of two units of data per clock period from a first input terminal, of four clock periods for the one-dimensional processing to initialize prior to the transposition and interchange the data of four clock periods for the two-dimensional processing to adjust its output sequence, a first register which receives via the first selector the data of the four clock period in the two-dimensional processing, a round-off/maximum limiting section which rounds in equally both positive and negative directions and maximum- limits the two-dimensional processing result input in every clock period from the register, a second register which is responsive to a control signal input from a second input terminal, updates in every clock period a register output of the round-off/maximum limiting section and saves the data of five clock

periods, a second selector which is responsive to a control signal input from a third input terminal and outputs the data saved in the second register in a reverse of the input sequence, a third selector which is responsive to a control signal input from the first input terminal and switches in every four block periods between an output of the round-off/maximum limiting section and an output of the second selector, and an output register which receives eight units of data at the rate of two units of data per clock period for four clock periods from the first register and outputs them at a rate of one data per clock period for eight clock periods.

14. The discrete cosine transformation/inverse discrete cosine transformation apparatus according to claim 10, wherein the N-point transformation processor incorporates a single eight-coefficient transformation section configured to switch in every eight coefficients between the one-dimensional processing and the two-dimensional processing and subject 8 × 8 coefficients of data to a discrete cosine transformation or an inverse discrete cosine transformation.

15. A discrete cosine transformation apparatus comprising:

an input processor which outputs data input one by one, at a rate of L data per clock period for M clock

periods;

an N-point transformation processor which N-point-transforms the data input at the rate of L data per clock period from the input processor and outputs the transformed data at the rate of L data per clock period;

an output processor which continuously outputs the one-dimensionally transformed data input at the rate of L data per clock period from the N-point transformation processor at the rate of L data per clock period for every M clock periods while rounding N two-dimensionally transformed data input at the rate of L data per clock period in the succeeding M clock periods; and

a transposition section which transposes N × N data input continuously at the rate of L data per clock period in every M clock periods and reading them continuously at the rate of L data per clock period in every M clock periods.

16. A discrete cosine transformation apparatus according to claim 15, wherein the input processor outputs the data at a rate of two data per clock period, and the N-point transformation processor eight-point transforms the data received at the rate of two data per clock period from the input processor and outputs the transformed data at the rate of two data per clock period.